REMARKS

Claims 1-8 are pending.

It is believed that this Amendment is fully responsive to the Office Action dated **January 30, 2002**.

Rejection Under 35 U.S.C. §102:

Claims 1-3 are rejected under 35 U.S.C. §102(b) as being anticipated by **Iwamoto (U.S. Patent No. 4,802,739)**.

In rejecting claims 1-3, the Examiner has stated that:

> " Regarding claim 1, Iwamoto discloses a power supply circuit with a circuit generating a positive polarity voltage (3 and the node connecting to terminal VDD; see column 2, lines 58-64), a terminal for outputting the positive voltage (VDD), a circuit generating a negative polarity voltage (3, the node connecting to terminal Vssi; see column 2, lines 58-64), a terminal for outputting the negative voltage (V_5S_2, when SW3 and SW4 are closed), and a short circuit for short circuiting the first and second terminals (5W5).
> Regarding claim 2, Iwamoto discloses that the switch may be a MOS transistor (column 9, lines 3-5). It is inherent that using its gate, a MOS transistor limits the current flowing through it.
> Regarding claim 3, Iwamoto discloses that the switch may be a MOS transistor (column 9, lines 3-5). A transistor is a switching element."

Even though the Office has artfully copied portions of the claimed invention and inserted at various locations parenthetical comments as to where the same element is alleged to be disclosed in the asserted prior art, the attempt is unfruitful, because the claimed invention is substantively different from Iwamoto. in Iwamoto, by short-circuiting both ends of the boosting capacitor C2 of the single boosting circuit 1, charges stored in the capacitor are discharged.

In contradistinction, in the present invention, the first circuit generates the positive polarity voltage and the second circuit generates the negative polarity voltage. By short-circuiting the positive polarity voltage outputting terminal and the negative polarity voltage outputting terminal, it is possible to efficiently discharge both charges stored in the capacitor of the first circuit and charges stored in the capacitor of the second circuit. Therefore, the present invention is entirely different from Iwamoto.

For reasons separate from the merit of the applied prior art, independent claim 1 has been further amended to better define features of the present invention, the added features are shown hereinbelow:

> " A power supply circuit, comprising:
> a first circuit for generating a positive polarity voltage, said first circuit including a rectifying circuit and a capacitor;
> a positive polarity voltage outputting terminal for outputting the positive polarity voltage from said first circuit;
> a second circuit for generating a negative polarity voltage;
> a negative polarity voltage outputting terminal for outputting the negative polarity voltage from said second circuit;
> a ground terminal for providing a reference potential for both of said positive polarity voltage and said negative polarity voltage; and
> a short circuit for short-circuiting substantially between said positive polarity voltage outputting terminal and said negative polarity voltage outputting terminal in response to a power-off signal, wherein residual charges of the capacitors pass said short circuit in turning a power off."

It is well settled that:

> "A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

Should the Office continue to assert that the claimed invention is anticipated by the prior art, a citation of where each and every element of the claimed invention that is disclosed in the prior art is respectfully requested.

It is respectfully submitted that independent claim 1, as amended, patentably distinguishes over the asserted prior art. All claims dependent thereon, by virtue of inherency, also patentably distinguish over the same prior art. Reconsideration and withdrawal of this rejection are respectfully requested.

Rejection Under 35 U.S.C. §103:

Claim 6 is rejected under 35 U.S.C. §103(a) as being unpatentable over **Iwamoto (U.S. Patent No. 4,802,739)** in view of **Sawanobori (JP No. 407336610)**.

In the outstanding Office action, it has been stated that "Iwamoto is silent with regard to using the power supply circuit with a CCD imager." The Applicant respectfully agrees with the Office assessed differentiation between the claimed invention and Iwamoto. However, that is not the only difference between Iwamoto and the claimed invention.

It should be noted that in Iwamoto, by short-circuiting both ends of the boosting capacitor C2 of the single boosting circuit 1, charges stored in the capacitor are discharged. In contradistinction, in the present invention, the first circuit generates the positive polarity voltage and the second circuit generates the negative polarity voltage. By short-circuiting the positive polarity voltage outputting terminal and the negative polarity voltage outputting terminal, it is possible to efficiently discharge both charges stored in the capacitor of the first circuit and charges stored in the capacitor of the

second circuit. Therefore, the present invention is entirely different from Iwamoto.

Furthermore, in Sawanobori, as to the control of voltage for CCD, when the negative value voltage is stopped being supplied, possible deterioration and destruction of the CCD is prevented by discharging the power source line S3 which supplied the negative value voltage; however, no discharge is performed on the power source line S2 which supplied the positive value voltage. Sawanobori is entirely different from Iwamoto in that Iwamoto includes only the single boosting circuit whereas Sawanobori is having two power source lines thus cannot be combined with Iwamoto.

Section 706.01(j) of the MPEP has specifically stated that:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claimed limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 466, 20 USPQ2d 1438 (Fed. Cir. 1991)"

It is respectfully submitted that the Office has not established a *prima facie* case of obviousness, because, 1) there is not any suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; 2) there is not any reasonable expectation of success in following the suggestion as stated in the outstanding Office action; 3) the teaching or suggestion to make the claimed combination and the reasonable expectation of success cannot both be found in the asserted prior art.

For the foregoing differences, independent claim 1, as amended, patentably distinguishes over the asserted prior art. All claims dependent thereon also patentably distinguish over the asserted prior art. Reconsideration and withdrawal of this rejection are respectfully requested.

Allowable Subject Matter:

The Examiner's early indication of allowable claims 4-5 and 7, is noted with appreciation.

New Claims

In response to the Office indication of allowable subject matter in claims 4-5 and 7, new independent claim 8 is submitted herewith. Independent claim 8 incorporates the subject matter of claims 1 and 4. Entry and allowance of newly submitted independent claim 8 are respectfully requested.

CONCLUSION

In view of the aforementioned amendments and accompanying remarks, all pending claims are believed to be in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully Submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

Michael N. Lau
Attorney for Applicant
Reg. No. 39,479

MNL/led
Atty. Docket No. **980673**
Suite 1000,1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

23850
PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made

H:\HOME\ldaugherty\MNL\98\980673\980673amendment.m

VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/082,581

IN THE SPECIFICATION:

Please amend the specification as follows:

-- Two circuits 24 and 26 are formed on a side of a secondary winding of the ~~transistor~~ transformer T. The circuit 24 functions as a first circuit to generate a positive-polarity voltage, e.g. 15V. The circuit 26 serves as a second circuit to create a negative polarity voltage, e.g. -7.5V. The voltage 15V generated by the first circuit 24 is outputted through a first terminal 24a to the CCD imager 14 of the camera 12 and the timing generator 16 for supplying various drive voltages to the CCD imager 14. The camera 12 further includes a clamp circuit 17. The voltage -7.5V generated by the second circuit 26 is outputted through a second terminal 26a to the CCD imager 14 and the timing generator 16. –

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A power supply circuit, comprising:

a first circuit for generating a positive polarity voltage, said first circuit including a rectifying circuit and a capacitor;

a ~~first~~ positive polarity voltage outputting terminal for outputting the positive polarity voltage from said first circuit;

a second circuit for generating a negative polarity voltage;

a ~~second~~ negative polarity voltage outputting terminal for outputting the negative polarity

voltage from said second circuit; ~~and~~

a ground terminal for providing a reference potential for both of said positive polarity voltage and said negative polarity voltage; and

a short circuit for short-circuiting substantially between said ~~first~~ positive polarity voltage outputting terminal and said ~~second~~ negative polarity voltage outputting terminal in response to a power-off signal, wherein residual charges of the capacitors pass said short circuit in turning a power off.

2. (Amended) A power supply circuit according to claim 1, wherein said short-circuit includes a series circuit having a switching element and a current-limiting element connected between said ~~first~~ positive polarity voltage outputting terminal and said ~~second~~ negative polarity voltage outputting terminal.

3. (Amended) A power supply circuit according to claim 1, wherein said short circuit includes a switching element connected between said ~~first~~ positive polarity voltage outputting terminal and said ~~second~~ negative polarity voltage outputting terminal.

4.(Amended) A power supply circuit according to claim 1, wherein said first circuit includes a chopper circuit for generating a low first positive voltage, and a fly-back circuit for receiving the first positive voltage from the chopper circuit to generate a high second positive voltage, ~~and further comprising:~~

said positive polarity voltage outputting terminal includes first and second output terminals for respectively outputting the first positive voltage and the second positive voltage~~;~~, and further comprising:

a diode connected between said first and second output terminals in a forward direction ~~of~~ from said first ~~positive voltage~~ output terminal to said second ~~positive voltage~~ output terminal.

7. (Amended) A camera, comprising:

a chopper circuit for generating a low first voltage;

a fly-back circuit for receiving the first voltage from said chopper circuit to generate a high second voltage;

first and second terminals for respectively outputting the first and second voltages;

a diode connected between said first terminal and said second terminal in a forward direction ~~of~~ from said first terminal to said second terminal; and

a CCD imager for receiving the positive polarity voltage and negative polarity voltage through said first terminal and said second terminal.